

Discipline:	Semester:-	Name of the Teaching Faculty:-
Electrical Engg.	5 <sup>TH</sup>	Pradeepta prajnananjan swain
Subject:-DIGITAL ELECTRONICS & MICROPROCESSOR [TH-1]	No of Days/per Week Class Allotted: 03	Semester-5 <sup>TH</sup> From:01.07.2026 To:05.11.2026 No of Weeks:-15
Week	Class/Day	Theory Topics
1st	1 <sup>st</sup>	<b>Digital Fundamentals Number Systems -</b> (1)Decimal, Binary. (2)Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3. (3)Gray, Alphanumeric codes, Boolean theorems.
	2 <sup>nd</sup>	(4)Logic gates and truth tables, Universal gates. (5)Sum of products and product of sums, Minterms' and Maxterms.
	3 <sup>rd</sup>	(6) Karnaugh map Minimization and QuineMcCluskey method of minimization (7) Karnaugh map Minimization and QuineMcCluskey method of minimization
2nd	1 <sup>st</sup>	<b>Combinational &amp; Synchronous Sequential Circuits-</b> (1)Design of Half and Full Adders, (2)Half and Full Subtractors. (3) Binary Parallel Adder –Multiplexer.
	2 <sup>nd</sup>	(4)Demultiplexers, Decoders, and Priority Encoder. (5) Flip flops – SR, JK, T, D, design of clocked sequential circuits – Design of Counters- Shift registers, Universal Shift Register.
	3 <sup>rd</sup>	(4)Demultiplexers, Decoders, and Priority Encoder. (5) Flip flops – SR, JK, T, D, design of clocked sequential circuits – Design of Counters- Shift registers, Universal Shift Register.
3rd	1 <sup>st</sup>	(4)Demultiplexers, Decoders, and Priority Encoder. (5) Flip flops – SR, JK, T, D, design of clocked sequential circuits – Design of Counters- Shift registers, Universal Shift Register
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	3 <sup>rd</sup>	(1)Design of Half and Full Adders, (2)Half and Full Subtractors. (3) Binary Parallel Adder –Multiplexer
4th	1 <sup>st</sup>	<b>8085 Processor</b> (1)Hardware Architecture. (2) pin diagram – Functional Building Blocks of Processor.
	2 <sup>nd</sup>	(1)Hardware Architecture. (2) pin diagram – Functional Building Blocks of Processor
	3 <sup>rd</sup>	(3)Memory organization – I/O ports and data transfer concepts. (4)Timing Diagram – Interrupts.
5th	1 <sup>st</sup>	(3)Memory organization – I/O ports and data transfer concepts. (4)Timing Diagram – Interrupts.
	2 <sup>nd</sup>	(3)Memory organization – I/O ports and data transfer concepts. (4)Timing Diagram – Interrupts.
	3 <sup>rd</sup>	(3)Memory organization – I/O ports and data transfer concepts. (4)Timing Diagram – Interrupts.
6th	1 <sup>st</sup>	<b>Programming Processor</b> (1)Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2)Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
	2 <sup>nd</sup>	(1)Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2)Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
	3 <sup>rd</sup>	(1)Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2)Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating

		modes.
7th	1st	(1) Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2) Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
	2nd	(1) Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2) Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
	3rd	(1) Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2) Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
8th	1st	(1) Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2) Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
	2nd	(1) Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2) Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
	3rd	(1) Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting (2) Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes.
9th	1st	<b>Asynchronous Sequential Circuits And Memory Devices</b> (1) Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments.
	2nd	(2) Hazards, Essential Hazards, Pulse mode sequential circuits.
	3rd	3) Design of Hazard free circuits. Basic memory structure – ROM -PROM EPROM – EEPROM EAPROM, RAM – Static and dynamic RAM.
10th	1st	(4) Programmable Logic Devices – Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA)
	2nd	(5) Doubt clearing class
	3rd	(5) class test.
11th	1st	<b>Digital Fundamentals Number Systems -</b> (1) Decimal, Binary. (2) Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3. (3) Gray, Alphanumeric codes, Boolean theorems.
	2nd	(4) Logic gates and truth tables, Universal gates. (5) Sum of products and product of sums, Minterms' and Maxterms.
	3rd	1) Design of Half and Full Adders.
12th	1st	(2) Half and Full Subtractors.
	2nd	(3) Binary Parallel Adder – Multiplexer.
	3rd	(3) Gray, Alphanumeric codes, Boolean theorems.
13th	1st	Doubt clearing class.
	2nd	Doubt clearing class.
	3rd	Doubt clearing class.
14th	1st	Doubt clearing class.
	2nd	Doubt clearing class.
	3rd	Class test.
15th	1st	Doubt clearing class.
	2nd	Doubt clearing class.

Pradeep Kumar Sanjan  
Sign. of faculty

~~24/06/26~~  
24/06/26  
Sign. of sr. lecturer

~~24/06/26~~  
24/06/26  
Sign. of principal

Head of Dept. (HOD)  
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